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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,448	12/31/2003	Se-Jun Kim	51876P552	9817

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,448	KIM ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9,11-13 and 19* is/are rejected.

7)☒ Claim(s) *4,8,10,14,18,20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31 December 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because reference numeral 800 in Fig. 9 is not correctly labeled as "voltage control oscillator" as described in the specification (page 23, line 14). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1, 4, 11, and 14 are objected to because of the following informalities:

Claim 1, lines 4-5, "a delay model for modeling delay time for buffering the external clock signal" should be changed to --for delaying a delayed clock signal-- (as shown in Fig. 5 and claimed limitation in lines 16-18 of claim 1);

Claim 1, lines 8-9, "an" should be changed to --a--;

Claim 1, line 20, "digital-analog converter" should be changed to -- analog-digital converter--;

Claim 4, line 2, "digital-analog converter" should be changed to -- analog-digital converter--;

Claim 11, lines 4-5, "a delay model for modeling delay time for buffering the external clock signal" should be changed to --for delaying a modulated signal-- (see claimed limitation in lines 17-19 of claim 11);

Claim 11, lines 9-10, "an" should be changed to --a--;

Claim 11, line 20, "digital-analog converter" should be changed to -- analog-digital converter--; and

Claim 14, line 2, "digital-analog converter" should be changed to -- analog-digital converter--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA), Fig. 3 in the present application, in view of Yahagi et al. (US Pat. 5,389,899).

With regard to claims 1, the admitted prior art, in instant Fig. 3, shows an analog DLL which buffers an external clock signal (CKIN) and uses the buffered clock signal as a reference clock signal (CKR), comprising a delay model (65); a phase comparator (75) for comparing a phase of the reference clock signal with a phase of an outputted signal from the delay model; a charge pump (80); a loop filter (90); a voltage control delay line (70) which delays the reference clock signal for a predetermined time, and outputs the delayed clock signal to the delay model, where the predetermined time is determined by the reference voltage. Fig. 3 of APA meets all the claimed limitations except for a tracking digital-analog converter (100 in instant Fig. 5) which converts the reference voltage to a digital value, and stores the digital value for keeping the reference voltage safely, and outputs a tracking voltage which corresponds to the digital value to the loop filter. Yahagi et al. teaches in Fig. 3 a circuit having a tracking digital-analog converter (9-13, 17, 114, 115, 130) as recited in the claim. Since Fig. 3 of and the APA are similar because they are frequency synthesizers, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement the tracking digital-analog converter taught by Yahagi et al. in order to save power consumption when the power saving mode is used.

With regard to claim 2, the tracking voltage is outputted to the loop filter during a standby mode (when switch 114 is ON).

With regard to claim 3, the loop filter (90 as shown in instant Figs. 3-4) includes a capacitor (C in instant Fig. 4) for storing the reference voltage.

With regard to claim 9, the references also meet the recited limitation in the claim.

5. Claims 11-13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA), Fig. 3 in the present application, in view of Yahagi et al., as applied to claims 1-3, and 9 above, and further in view of Nogami (US Pat. 6,774,679).

With regard to claim 11, the above discussed the analog phase locked loop circuit of the references meets all of the claimed limitations except that the frequency generator is a voltage control oscillator instead of a voltage control delay line as recited in the claim. Nogami teaches in Figs. 6-12 a phase locked loop circuit having a voltage control delay line (20), which can be replaced by a voltage control oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to replace of the voltage control delay line in the analog phase locked loop of the references with the voltage control oscillator as taught by Nogami in order to meet the specific condition of the particular application.

Claims 12, 13, and 19 are similar rejected; note the above discussion with regard to claims 2, 3, and 9.

Allowable Subject Matter

6. Claims 4-8, 10, 14-18, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest an analog DLL circuit (as shown in Fig. 5), as recited in claims 4 and 14, having a very specific limitation as the tracking analog-digital converter (100 in instant Fig. 6) includes a voltage comparator (110) for comparing the reference voltage (VC) with the tracking voltage (VT); a counting means (120) for counting in response to an outputted signal (UP1, DOWN1) from the voltage comparator, and for outputting an counting signal; a register (130) for storing a digital value which corresponds to the counting signal; and an digital-analog converting means (140, 160) for generating a voltage which corresponds to the digital value, and for outputting the voltage as the tracking voltage (VT); and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pyeon et al. (US 6,392,456) is cited as of interest because it discloses an analog mixed digital DLL circuitry.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
February 21, 2005

TIMOTHY P. CALLAHAN
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